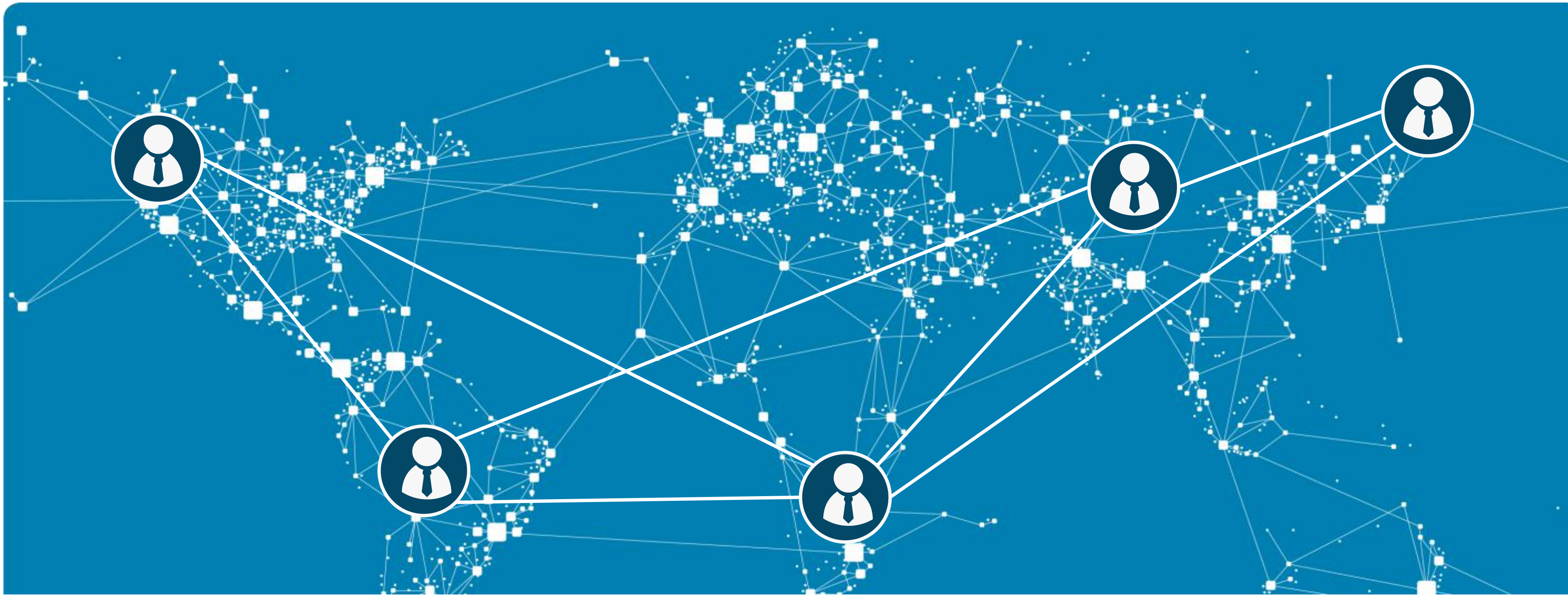

周报告

宋金林　导师：李仁发教授

○论文进度：完成初稿（7页）

An Efficient Scheduling Method of Energy Consumption Constrained Parallel Applications on Heterogeneous Systems

Jinlin Song, Guoqi Xie*, Renfa Li
College of Computer Science and Electronic Engineering, Hunan University,
Key Laboratory for Embedded and Network Computing of Hunan Province, China
{songjinlin@hnu.edu.cn, xgqman@hnu.edu.cn, lirenfa@hnu.edu.cn }
*Corresponding author

Abstract—As the explosive growth of energy consumption in current heterogeneous parallel and distributed systems, energy consumption constraint have been one of the primary design issues. Minimizing the schedule length while satisfying the energy consumption constraint of an application is one of the most important problem which have been studied recently. Previous methods tried to presuppose the minimum energy consumption assignment for each task to minimize the schedule length of energy consumption constrained applications on heterogeneous parallel and distributed systems based on the dynamic voltage and frequency scaling (DVFS) technique. However, the preassignment of tasks with the minimum energy consumption does not necessarily lead to the minimization of the schedule length. In this study, we propose an efficient scheduling algorithm using an equilibrium strategy to preassign the given energy and select processors. The results of experiments on several real parallel applications validate that the proposed algorithm can obtain shorter schedule lengths while meet the need of energy consumption constraints compared with the state-of-the-art methods in various situations.

Keywords—energy consumption constraint, dynamic voltage and frequency scaling (DVFS), heterogeneous systems, Parallel application.

I. INTRODUCTION

A. Background

The emergence and development of heterogeneous distributed system is to meet the needs of intensive large-scale scientific computing and commercial

DPM turns the idle components off leading the resources to the hibernate mode to reduce the energy consumption so it only works when the idle time is long enough. In this study, DVFS technologies is adopted, which achieves energy-efficient optimization by simultaneously scaling down the supply voltage and frequency of a processor.

B. Motivation

The problem of minimizing the schedule length of an energy consumption application with precedence-constrained tasks has been solved in a number of studies [2], [8], [12]. However, the first two studies [2], [8] only focus on homogeneous systems. Xiao et al. [12] solved the same problem for heterogeneous systems by presupposing tasks with the minimum energy consumption to satisfy the energy consumption constraint of the application, however, preassigning the minimum energy consumption to each task is not effective while the given energy consumption is little because the tasks with low priority have to select the processor with the minimum execution cost, which will lead to longer schedule length. Therefore, a more efficient scheduling method is needed.

The rest of this paper is organized as follow. Section 2 reviews related studies. Section 3 presents related models and preliminaries. Sections 4 describe the problem and propose the ESECC algorithms. Section 5 verifies the ESECC algorithms and Section 6 concludes this study.

II. RELATED WORKS

Energy consumption optimization using DVFS technology has attracted much attention since 1990 [3] when the energy consumption optimization for

strategies for those systems have been proposed. The problems of minimizing the expected energy consumption on homogeneous multiprocessor with precedence constrained tasks have been presented in [13], [14], for heterogeneous distributed systems has been studied in [9], [10], [15]. In this paper, we consider a parallel application in heterogeneous distributed computing system. Huang et al. [9] proposed enhanced energy-efficient scheduling (EES) algorithm to reclaim the slack time for each task on the same processor through an "upward" approach. Moreover, Tang et al. [10] studied the same problem through merging the relatively inefficient processors by reclaiming the slack time to reduce energy dissipation, but it will increases the time complexity. A new method combining "downward" and "upward" approaches was presented to implement low time-complexity energy consumption minimization [15]. However, the aforementioned studies mainly managing the slack time to reduce energy consumption. But those studies mainly consider minimizing the energy consumption while meeting the deadline of the parallel applications. Lee et al. [7] presented two energy-conscious scheduling (ECS and ECS + idle) heuristics to explore the trade off of the schedule length and energy consumption for parallel tasks on heterogeneous distributed systems. Xiao et al. [12] aiming at minimizing the schedule length of a parallel application with energy consumption constrained in heterogeneous distributed systems which is decomposed into two sub-problems, namely, satisfying the energy consumption constraint and minimizing the schedule length. The proposed algorithm (MSLECC) achieves a minimum schedule length while satisfied a given system energy consumption, but the results is too pessimism. In this paper, we study the same problem by introduce a low bound of energy consumption for each task to implement a tight schedule length while meet the energy consumption constraint.

III. MODELS AND PRELIMINARIES

A. Application model

In this work, we assume that the system consists of a set heterogeneous processors: $U = \{u_1, u_2, \ldots, u_{|U|}\}$, where $|U|$ denotes the size of set U. The parallel application can be represented by a DAG as shown in Fig.1. Let $G = \{N, W, M, C\}$. N represents a set of nodes in G: $N = \{n_i\}$, each node means a task which has different worst case execution times (WCETs) on different processors. W is an $|N| \times |U|$ matrix where $w_{i,k}$ represents the WCET of n_i

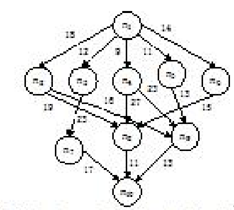

Fig.1 A simple example of DAG-based parallel application

Considering the example of a DAG shows in Fig.1. An application consists of ten tasks and executed on three processors. The WCET for each task on different processors with the maximum frequency is shown in Table 1. Such as n_1 has an execution time 14, 16, 9 while n_1 assigned to u_1, u_2, u_3, respectively. The weight 18 on the edge between n_1 and n_2 in Fig.1 represents the communication time denoted by $c_{1,2}$.

B. Energy model

The power consumption of CMOS circuits are consists of static and dynamic energy consumption denoted [illegible] and [illegible] respectively, and the supply voltage and operating frequency for CMOS circuits is nearly linear relationship so that we can change the operating frequency to optimize energy consumption. In this work, we adopt the system-level power model common used in [17]-[19], where the power consumption for a DVFS-enable system with frequency f is given by:

$$P(f) = P_s + h(P_{ind} + P_d) = P_s + h(P_{ind} + C_{ef} f^m) \quad (1)$$

P_s is the static power and the dynamic power is composed of two parts: P_{ind} and P_d. P_{ind} is the frequency-independent dynamic power which is a constant. P_d is the frequency-dependent dynamic power which is varies according to the frequency. h represents the system state where $h = 1$ means the system is active, otherwise the system is turned off and $h = 0$. C_{ef} is effective switching capacitance and m is the dynamic power exponent.

The static power is unmanageable and is not the main factor, we ignore it in this paper and mainly considering the dynamic part. While we slow down the processing frequencies, the execute time of tasks would increase simultaneously so that lower frequencies may

C类会议

General Information

- Home
- Proceedings & Special Issues
- Important Dates
- Paper Submission

ISPA 2017 Committees

- General Chairs
- Program Committee
- Steering Chairs
- Workshop Chairs
- Publicity Chairs
- Publication Chair
- Registration Chair
- Organizing Chairs
- Webmaster

ISPA 2017 Details

- Hotel Reservation
- Tour Reservation
- Visa Information & Invitation Letter
- Call for Papers

NEWS

The IEEE ISPA 2017 conference website is opening on December 31, 2016. NEW

The 15th IEEE International Symposium on Parallel and Distributed Processing with Applications (IEEE ISPA 2017)
Guangzhou, China, December 12-15, 2017

Organizers:
Guangzhou University, China
Central South University, China

http://trust.gzhu.edu.cn/conference/ISPA2017/

Call for Participation

Welcome to participate in IEEE ISPA 2017, Guangzhou, China, December 12-15, 2017! Guangzhou, a city in spring forever, is the capital city of Guangdong Province. Guangzhou is also the third largest city in China, located in the north of the Pearl River Delta, close to Hong Kong and Macau. With evergreen plants and flowers blooming all year round, the city has an alias of "City of Flowers". Guangzhou is one of the first batch of 24 historical and cultural cities released by the State Council, with more than 2200 years of history and profound cultural heritage, and also a major terminus of the maritime Silk Road. Guangzhou is one of the most famous tourist resorts in China, with a lot of tourist sites, such as Baiyun Mountain, Guangzhou Tower, and Yuexiu Park.

接下来任务

- 论文还需要些修改，还需用Latex排版。

THANKS